CY7C1041DV33

4 Mbit (256K x 16) Static RAM

Features

- Pin and function compatible with CY7C1041CV33
- High speed
  - t_{AA} = 10 ns
- Low active power
  - I_{CC} = 90 mA at 10 ns (industrial)
- Low CMOS standby power
  - I_{SB2} = 10 mA
- 2.0V data retention
- Automatic power down when deselected
- TTL compatible inputs and outputs
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features
- Available in Pb-free 48-ball VFBGA, 44-pin (400-mil) molded SOJ, and 44-pin TSOP II packages

Functional Description

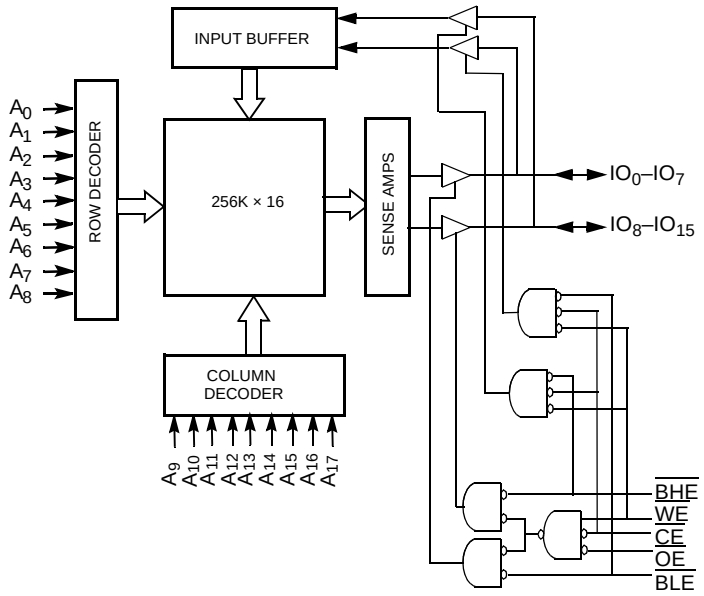
The CY7C1041DV33[1] is a high performance CMOS Static RAM organized as 256K words by 16 bits. To write to the device, take Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte LOW Enable ($\overline{BLE}$) is LOW, then data from IO pins (IO_0 to IO_7) is written into the location specified on the address pins (A_0 to A_{17}). If Byte HIGH Enable ($\overline{BHE}$) is LOW, then data from IO pins (IO_8 to IO_{15}) is written into the location specified on the address pins (A_0 to A_{17}).

To read from the device, take Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If $\overline{BLE}$ is LOW, then data from the memory location specified by the address pins appears on IO_0 to IO_7. If $\overline{BHE}$ is LOW, then data from memory appears on IO_8 to IO_{15}. See the Truth Table on page 9 for a complete description of read and write modes.

The input and output pins (IO_0 to IO_{15}) are placed in a high impedance state when the device is deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), $\overline{BHE}$ and $\overline{BLE}$ are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW and $\overline{WE}$ LOW).

The CY7C1041DV33 is available in a standard 44-pin 400-mil wide SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout and a 48-ball fine-pitch ball grid array (FBGA) package.

Logic Block Diagram



Note
1. For guidelines on SRAM system design, refer to the “System Design Guidelines” Cypress application note, available at www.cypress.com.

Selection Guide

Description	–10 (Industrial)	–12 (Automotive)[2]	Unit
Maximum Access Time	10	12	ns
Maximum Operating Current	90	95	mA
Maximum CMOS Standby Current	10	15	mA

Pin Configuration

Figure 1. 44-Pin SOJ/TSOP II

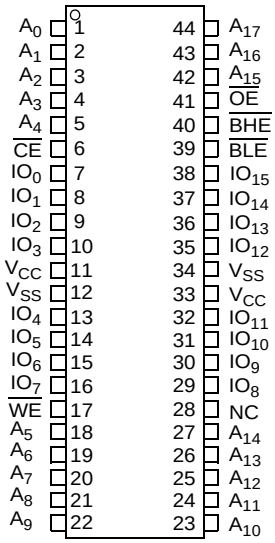


Figure 2. 48-Ball VFBGA (Pinout 1) [3, 4]

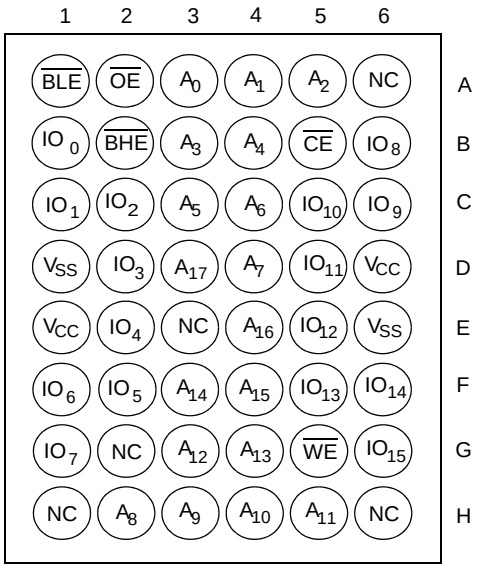
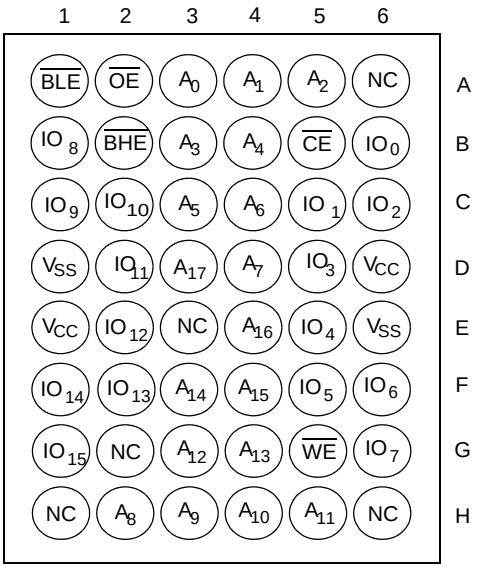


Figure 3. 48-Ball VFBGA (Pinout 2) [3, 4]



Notes
2. Automotive product information is Preliminary.
3. NC pins are not connected on the die.
4. Pinout 1 is compliant with CY7C1041CV33 and pinout 2 is JEDEC compliant. The difference between the two is that the higher and lower byte IOs ($IO_{[7:0]}$ and $IO_{[15:8]}$ balls) are swapped.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage on V_{CC} Relative to GND [5] ....–0.3V to +4.6V

DC Voltage Applied to Outputs in High-Z State [5] ..... –0.3V to V_{CC} +0.3V

DC Input Voltage [5] ..... –0.3V to V_{CC} +0.3V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... .....>2001V (MIL-STD-883, Method 3015)

Latch Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}	Speed
Industrial	–40°C to +85°C	3.3V ± 0.3V	10 ns
Automotive	–40°C to +125°C	3.3V ± 0.3V	12 ns

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		–10 (Industrial)		–12 (Automotive)		Unit
				Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}[5]	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}[5]	Input LOW Voltage			–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max, f = f_{MAX} = $1/t_{RC}$	100 MHz		90		-	mA
			83 MHz		80		95	mA
			66 MHz		70		85	mA
			40 MHz		60		75	mA
I_{SB1}	Automatic CE Power Down Current—TTL Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			20		25	mA
I_{SB2}	Automatic CE Power Down Current—CMOS Inputs	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0			10		15	mA

Note

5. Minimum voltage is –2.0V and V_{IH}(max) = V_{CC} + 2V for pulse durations of less than 20 ns.

Capacitance[6]

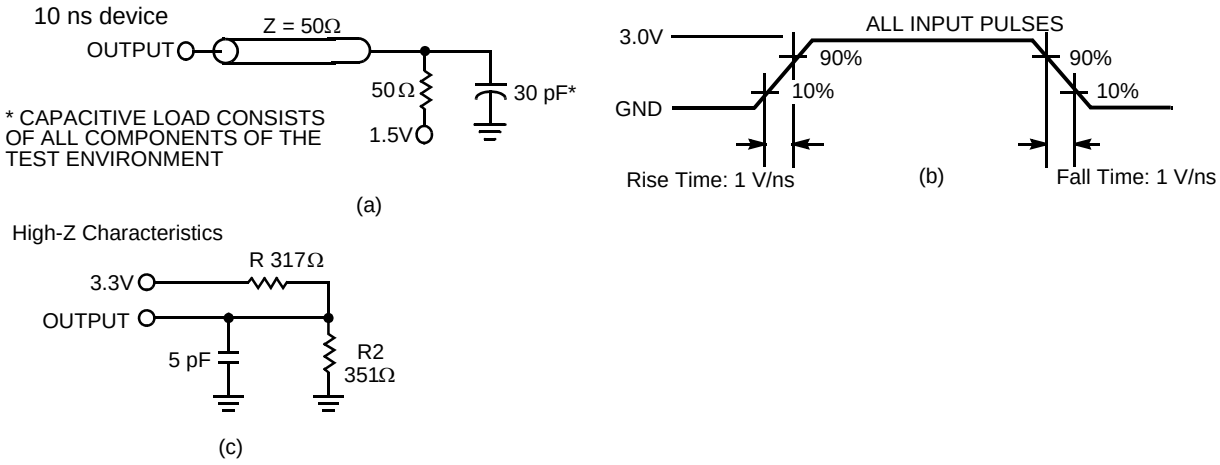
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	IO Capacitance		8	pF

Thermal Resistance[6]

Parameter	Description	Test Conditions	FBGA Package	SOJ Package	TSOP II Package	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, four layer printed circuit board	27.89	57.91	50.66	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		14.74	36.73	17.17	°C/W

AC Test Loads and Waveforms

The AC test loads and waveform diagram follows.[7]



Notes

6. Tested initially and after any design or process changes that may affect these parameters.
7. AC characteristics (except High-Z) are tested using the load conditions shown in AC Test Loads and Waveforms (a). High-Z characteristics are tested for all speeds using the test load shown in (c).

AC Switching Characteristics Over the Operating Range[8]

Parameter	Description	–10 (Industrial)		–12 (Automotive)		Unit
		Min	Max	Min	Max	
Read Cycle						
t_{power}[9]	V_{CC}(Typical) to the First Access	100		100		µs
t_{RC}	Read Cycle Time	10		12		ns
t_{AA}	Address to Data Valid		10		12	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		10		12	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		5		6	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z	0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[10, 11]		5		6	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[11]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[10, 11]		5		6	ns
t_{PU}	$\overline{CE}$ LOW to Power Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power Down		10		12	ns
t_{DBE}	Byte Enable to Data Valid		5		6	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		ns
t_{HZBE}	Byte Disable to High-Z		6		6	ns
Write Cycle[12, 13]						
t_{WC}	Write Cycle Time	10		12		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	7		8		ns
t_{AW}	Address Setup to Write End	7		8		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Setup to Write Start	0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	7		8		ns
t_{SD}	Data Setup to Write End	5		6		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[11]	3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[10, 11]		5		6	ns
t_{BW}	Byte Enable to End of Write	7		8		ns

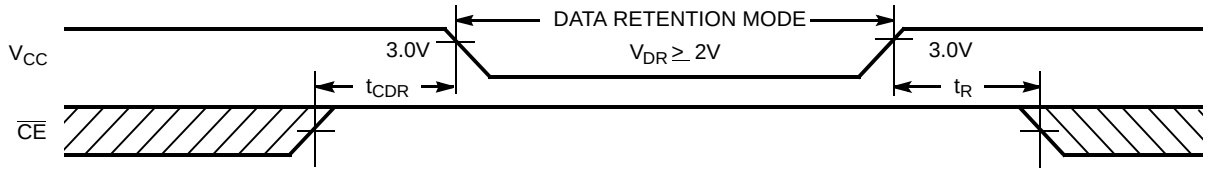
Notes

8. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
9. t_{POWER} gives the minimum amount of time that the power supply should be at typical V_{CC} values until the first memory access is performed.
10. t_{HZOE}, t_{HZCE}, t_{HZBE} and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads and Waveforms. Transition is measured when the outputs enter a high impedance state.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, t_{HZBE} is less than t_{LZBE}, and t_{HZWE} is less than t_{LZWE} for any given device.

Data Retention Characteristics Over the Operating Range

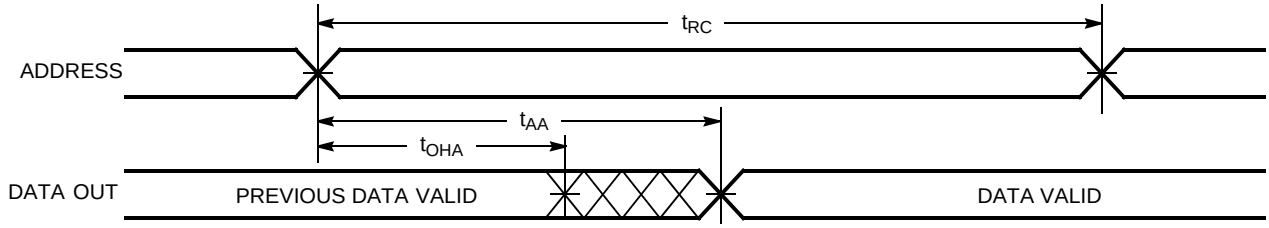
Parameter	Description	Conditions[14]		Min	Max	Unit
V_{DR}	V_{CC} for Data Retention			2.0		V
I_{CCDR}	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$	Ind'l		10	mA
			Auto		15	mA
t_{CDR}[6]	Chip Deselect to Data Retention Time			0		ns
t_R[15]	Operation Recovery Time			t_{RC}		ns

Data Retention Waveform



Switching Waveforms

Figure 4. Read Cycle No. 1[16, 17]



Notes

12. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write and the transition of either of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.
13. The minimum write cycle time for Write Cycle No. 4 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
14. No input may exceed V_{CC} + 0.3V.
15. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min.)} \geq 50$ µs or stable at $V_{CC(min.)} \geq 50$ µs.
16. Device is continuously selected. $\overline{OE}$, $\overline{CE}$, $\overline{BHE}$, and $\overline{BHE}$ = V_{IL}.
17. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled)[17, 18]

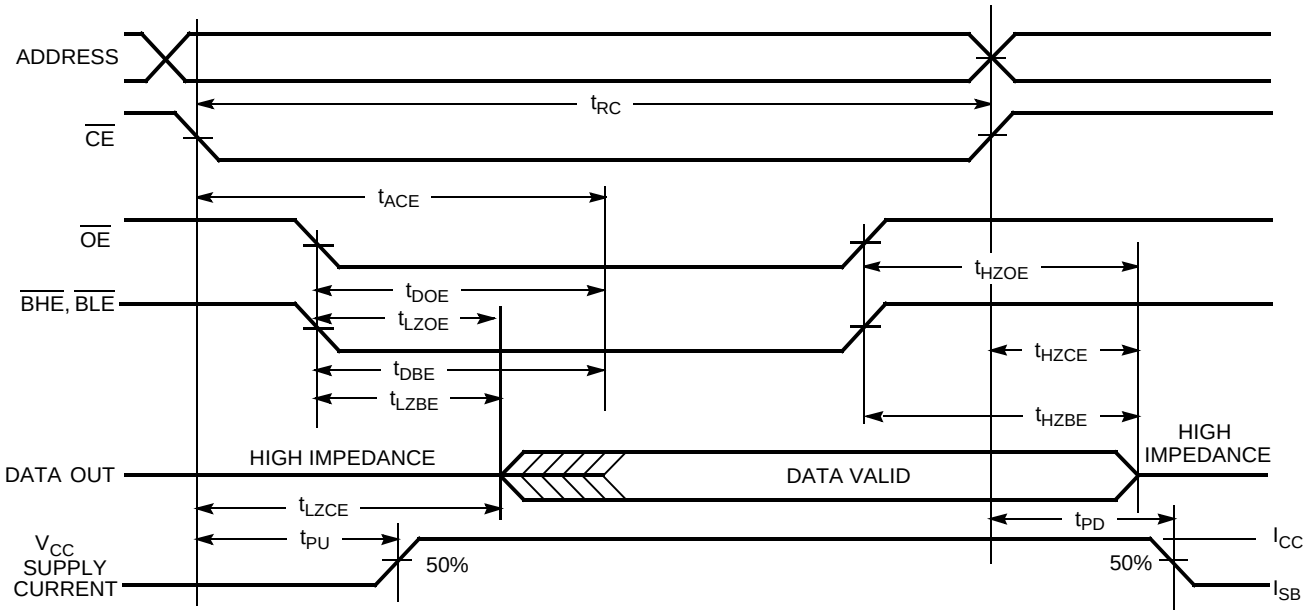
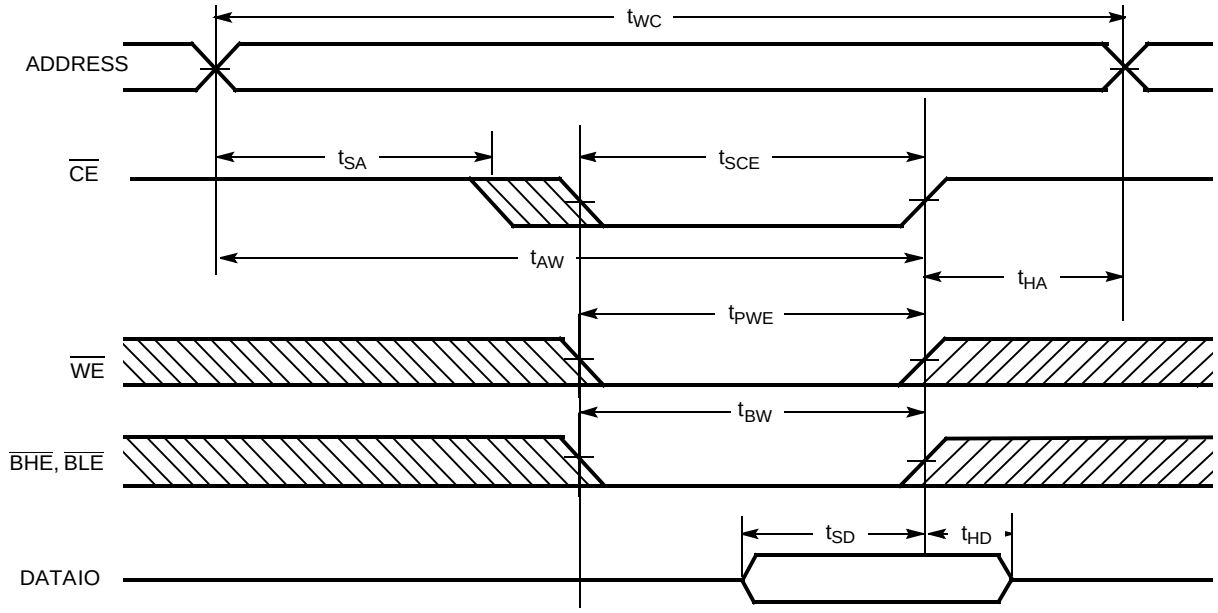


Figure 6. Write Cycle No. 1 ($\overline{CE}$ Controlled)[19, 20]



Notes
18. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
19. Data IO is high impedance if $\overline{OE}$ or $\overline{BHE}$ and $\overline{BLE}$ = V_{IH}.
20. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 ($\overline{BLE}$ or $\overline{BHE}$ Controlled)

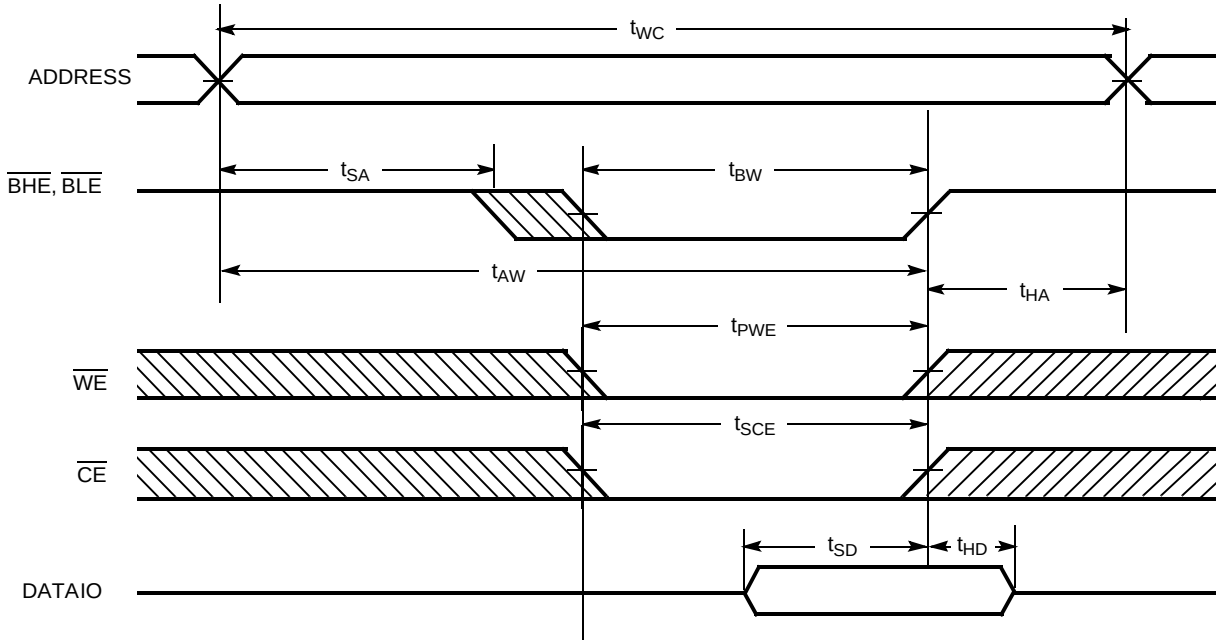
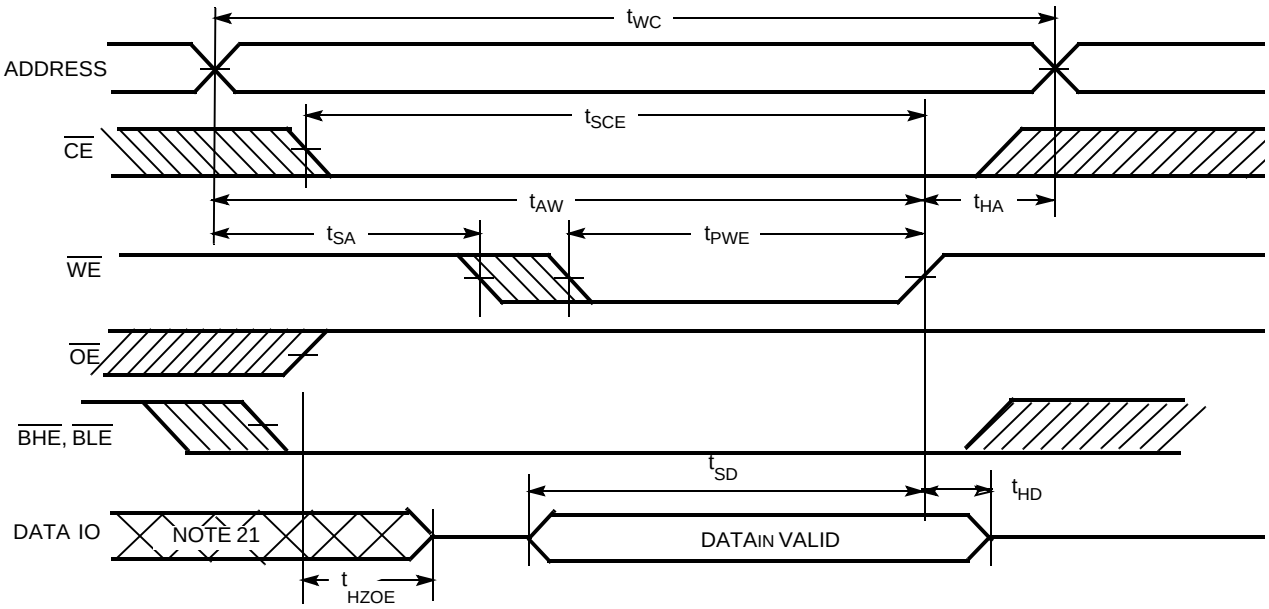


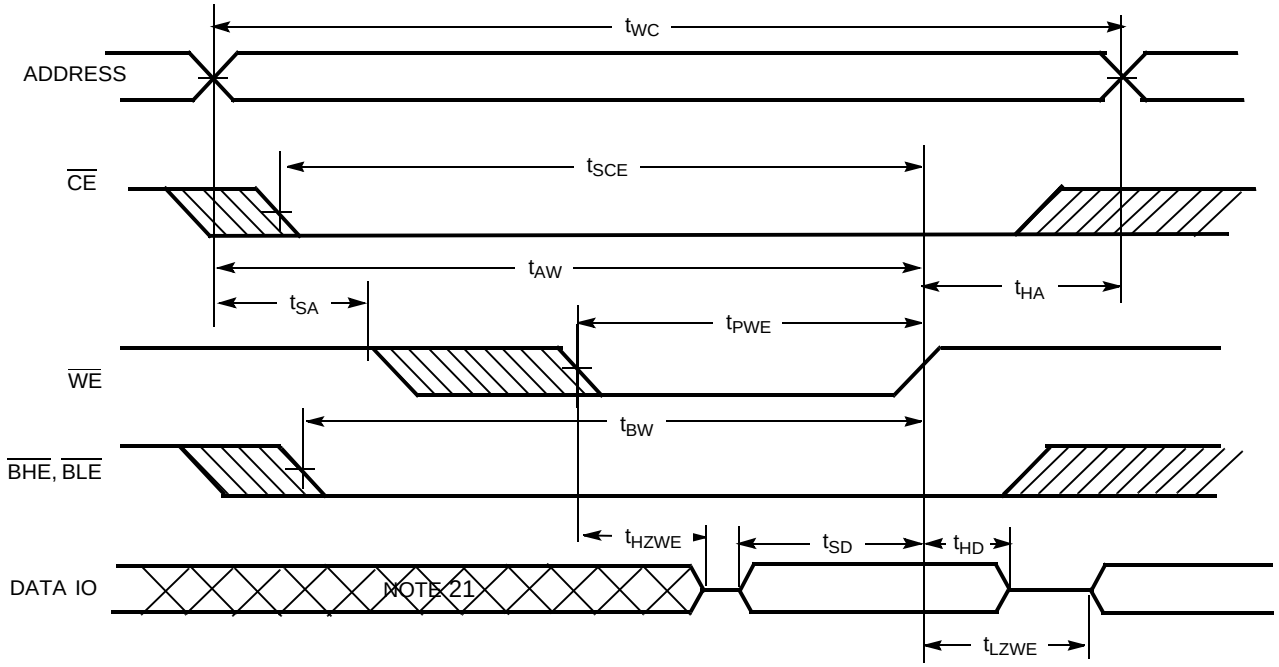
Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[19, 20]



Note
21. During this period the IOs are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 4 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{BLE}$	$\overline{BHE}$	IO_0–IO_7	IO_8–IO_{15}	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power Down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read All Bits	Active (I_{CC})
L	L	H	L	H	Data Out	High-Z	Read Lower Bits Only	Active (I_{CC})
L	L	H	H	L	High-Z	Data Out	Read Upper Bits Only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write All Bits	Active (I_{CC})
L	X	L	L	H	Data In	High-Z	Write Lower Bits Only	Active (I_{CC})
L	X	L	H	L	High-Z	Data In	Write Upper Bits Only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

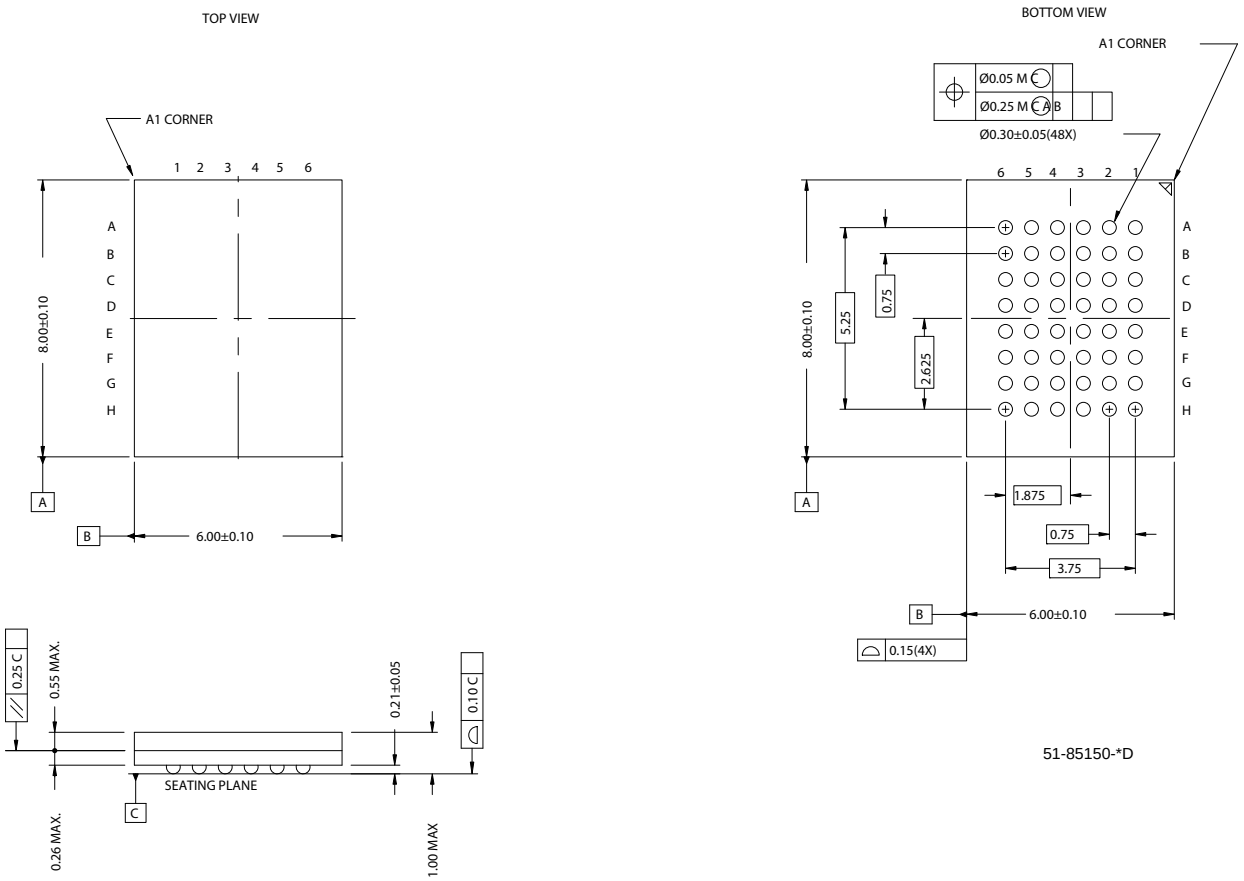
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1041DV33-10BVI	51-85150	48-Ball VFBGA	Industrial
	CY7C1041DV33-10BVXI		48-Ball VFBGA (Pb-Free) Pinout - 1 [4]	
	CY7C1041DV33-10BVJXI		48-Ball VFBGA (Pb-Free) Pinout - 2 [4]	
	CY7C1041DV33-10VXI	51-85082	44-Pin (400-mil) Molded SOJ (Pb-Free)	
	CY7C1041DV33-10ZSXI	51-85087	44-Pin TSOP II (Pb-Free)	
12	CY7C1041DV33-12BVXE	51-85150	48-Ball VFBGA (Pb-Free)	Automotive
	CY7C1041DV33-12VXE	51-85082	44-Pin (400-mil) Molded SOJ (Pb-Free)	
	CY7C1041DV33-12ZSXE	51-85087	44-Pin TSOP II (Pb-Free)	

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

Figure 10. 48-Ball VFBGA (6 x 8 x 1 mm) (51-85150)



Package Diagrams(continued)

Figure 11. 44-Pin (400-mil) Molded SOJ (51-85082)

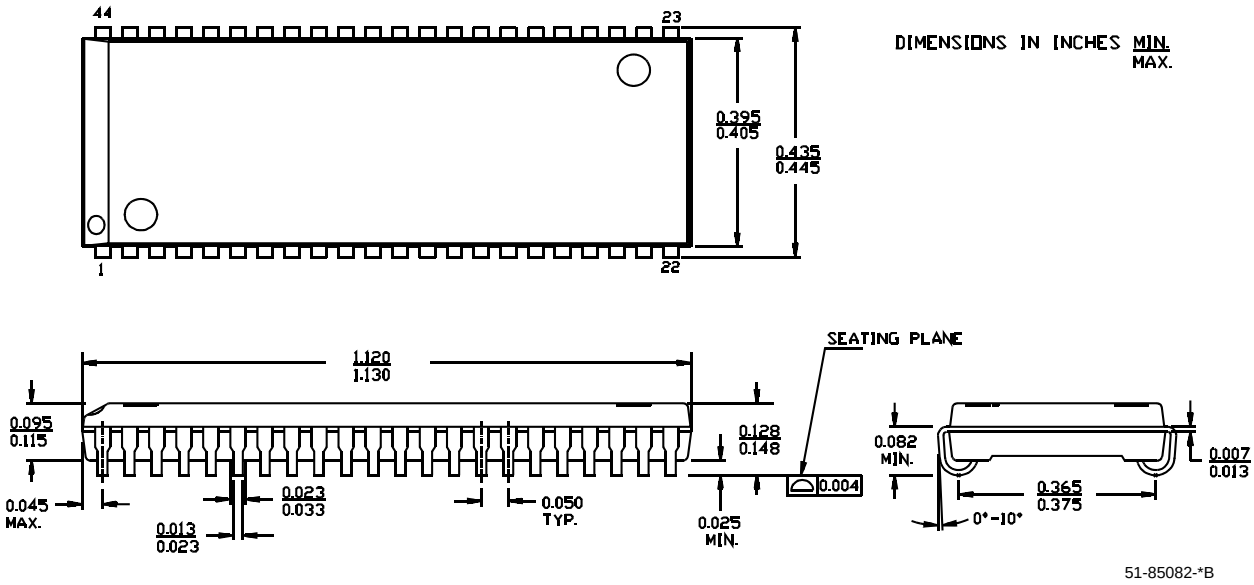
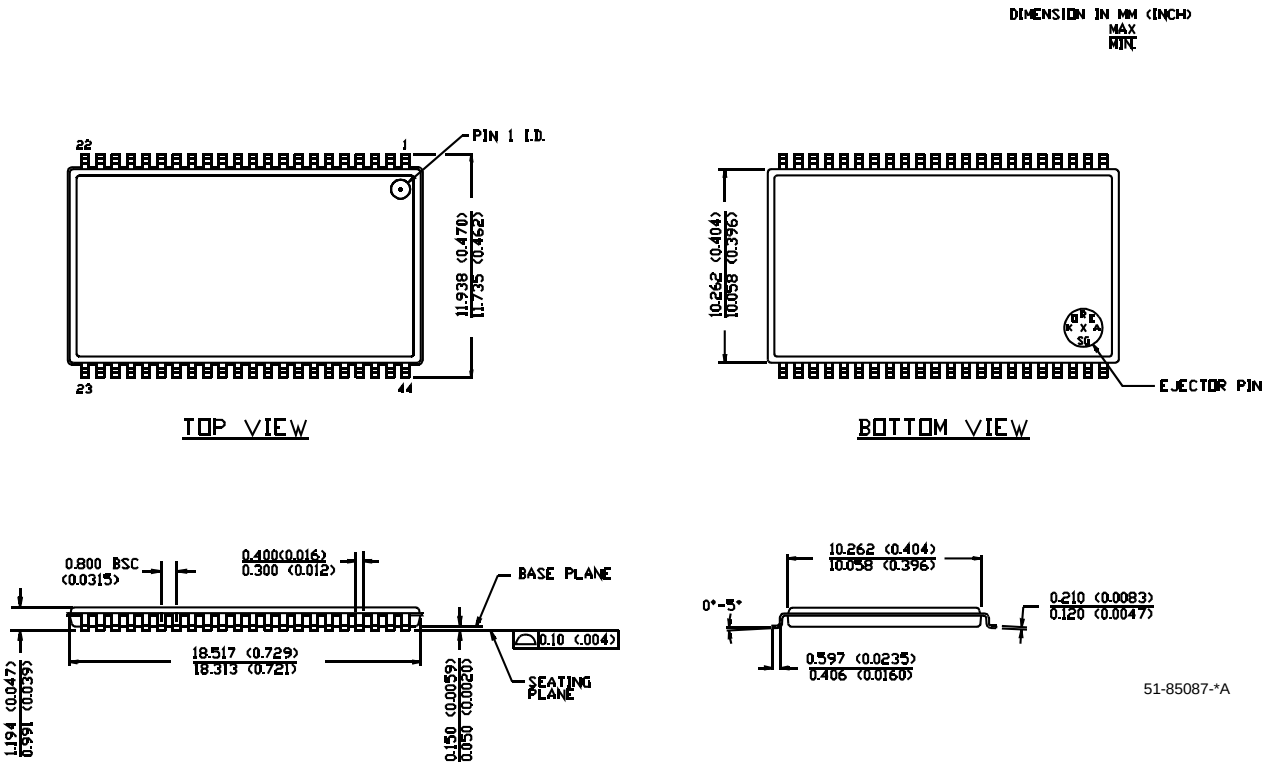


Figure 12. 44-Pin TSOP II (51-85087)



Document History Page

Document Title: CY7C1041DV33 4 Mbit (256K x 16) Static RAM Document Number: 38-05473				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	201560	SWI	See ECN	Advance Data sheet for C9 IPP
*A	233729	RKF	See ECN	1.AC, DC parameters are modified as per EROS(Spec # 01-2165) 2.Pb-free offering in the 'Ordering information'
*B	351117	PCI	See ECN	Changed from Advance to Preliminary Removed 15 and 20 ns Speed bin Corrected DC voltage (min) value in maximum ratings section from - 0.5 to - 0.3V Redefined I_{CC} values for Com'l and Ind'l temperature ranges I_{CC} (Com'l): Changed from 100, 80 and 67 mA to 90, 80 and 75 mA for 8, 10 and 12ns speed bins respectively I_{CC} (Ind'l): Changed from 80 and 67 mA to 90 and 85 mA for 10 and 12ns speed bins respectively Added Static Discharge Voltage and latch-up current spec Added $V_{IH(max)}$ spec in Note# 2 Changed Note# 4 on AC Test Loads Changed reference voltage level for measurement of Hi-Z parameters from ±500 mV to ±200 mV Added Data Retention Characteristics/Waveform and footnote # 11, 12 Added Write Cycle (WE Controlled, OE HIGH During Write) Timing Diagram Changed Package Diagram name from 44-Pin TSOP II Z44 to 44-Pin TSOP II ZS44 and from 44-Pin (400-mil) Molded SOJ V34 to 44-Pin (400-mil) Molded SOJ V44 Changed part names from Z to ZS in the Ordering Information Table Added 8 ns Product Information Added Pin-Free Ordering Information Shaded Ordering Information Table
*C	446328	NXR	See ECN	Converted from Preliminary to Final Removed -8 speed bin Removed Commercial Operating Range product information Included Automotive Operating Range product information Updated Thermal Resistance table Updated footnote #8 on High-Z parameter measurement Updated the ordering information and replaced Package Name column with Package Diagram in the Ordering Information Table
*D	480177	VKN	See ECN	Added -10BVI product ordering code in the Ordering Information table
*E	2541850	VKN/PYRS	07/22/08	Added -10BVJXI part

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